◆ FEATURES

- High accuracy, less than 0.1% error over a dynamic range of 6000:1
- High stability, less than 0.1% error in the output frequency fluctuation
- Measure the active power in the positive orientation and negative orientation, transform to fast pulse output(CF)
- Provide two current input for line and neutral current measurement
- Mesure instantaneous IRMS and VRMS over a dynamic range of 3000:1
- Provide SAG detection and Phase failure detection
- On-chip power supply detector
- On-chip anti-creep protection with the programmable threshold set
- Provide the pulse output with programmable frequency adjustment
- Provide the programmable gain adjustment and phase compensation
- Measure the power factor (PF)
- Provide a programmable interrupt request signal (/IRQ)
- Provide a UART communication interface
- On-chip voltage reference of 2.5V
- With 3.58MHz external crystal oscillator
- Single 5V supply, 25mW (typical)

Interralated patents are pending

◆ DESCRIPTION

The BL6523GX is a low cost, high accuracy, high stability, electrical energy measurement IC intended to single phase, multifucion applications.

The BL6523GX incorporates three high accuracy Sigma-Delta ADC, voltage reference, power management and digital signal processing circuit using to calculates active energy, apparent energy, IRMS, VRMS etc.

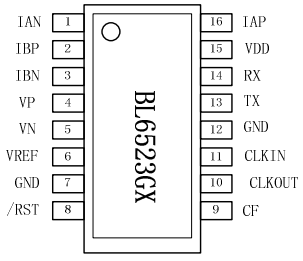
The BL6523GX have two current input for line and neutral current measurement, when these currents differ by more than the programmable Fault threshold value(RMS or WATT), the BL6523GX give the tamper detection and can enable neutral current billing,

The BL6523GX measures line voltage, current and calculates active, apparent energy, power factor, line frequency, detect sag, overvoltage, overcurrent, peak, and reverse power, zero-crossing voltage.

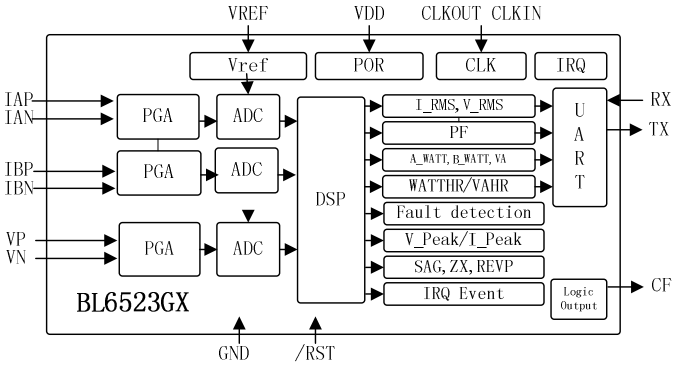
The BL6523GX provides access to on-chip meter registers via UART communication interface.

The BL6523GX provide all-digital domain offset compensation, gain adjustment, phase compensation (maximum ±2.54° adjustable) .

◆ BLOCK DIAGRAM



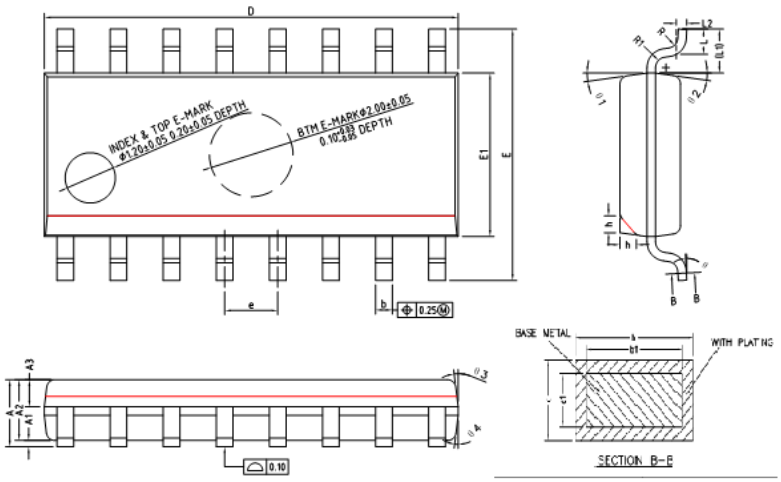
SOP16



PIN DESCRIPTIONS（SOP16）

Pin	Symbol	DESCRIPTIONS
16,1	IAP,IAN	Analog input for current channel A, These inputs are fully differential voltage inputs with a maximum signal range of ±660 mV, the PGA accociated with these inputs has a maximum gain of 32.
2,3	IBP，IBN	Analog input for current channel A, These inputs are fully differential voltage inputs with a maximum signal range of ±660 mV, the PGA accociated with these inputs has a maximum gain of 32.
4,5	VP，VN	Analog Input for Voltage Channel. These inputs are fully differential voltage inputs with a maximum signal range of ±660 mV, the PGA accociated with these inputs has a maximum gain of 32.
6	VREF	On-Chip Voltage Reference. The on-chip reference has a nominal value of 2.5V ± 8% and a typical temperature coefficient of 30ppm/℃. This pin should be decoupled with a 0.1uF ceramic capacitor. An external reference source may also be connected at this pin.
7	GND	Ground Reference.
8	/RST	Reset Pin. Logic low on this pin will hold the ADCS and digital circuitry in a reset condition and clear internal registers.
9	CF	Calibration Frequency. The CF logic output gives instantaneous real power information. This output is intended to use for calibration purposes. The full-scale output frequency can be scaled by the value of WA_CFDIV register. When the power is low, the pulse width is equal to 90ms. When the power is high and the output period less than 180ms, the pulse width equals to half of the output period.
10	CLKOUT	A crystal can be connected across this pin and Pin11 as described above to provide a clock source.
11	CLKIN	Clock Input for BL6523GX. An external clock can be provided at this logic input, Alterrnatively, a crystal (3.58MHz) can be connected across this pin and pin10 to provide a clock source.
12	GND	Ground Reference.
13	TX	Data output for UART interface.
14	RX	Data input for UART interface.
15	VDD	Power Supply（+5V）,provides the supply voltage for BL6523GX. It should be maintained at +4.75V~+5.25V for specified operation

◆ Package Dimensions(SOP-16)



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.75
A1	0.10	0.15	0.25
A2	1.35	1.45	1.55
A3	0.55	0.65	0.75
b	0.36	–	0.51
b1	0.35	0.40	0.45
c	0.18	–	0.25
c1	0.17	0.20	0.23
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.22	1.27	1.32
L	0.45	0.60	0.80
L1		1.04REF	
L2		0.25BSC	
R	0.07	–	–
R1	0.07	–	–
h	0.30	0.40	0.50
θ	0°	–	8°
θ1	6°	8°	10°
θ2	6°	8°	10°
θ3	5°	7°	9°
θ4	5°	7°	9°

◆ ABSOLUTE MAXIMUM RATIONS

（T = 25 ℃）

Parameter	Symbol	Value	单位
Power Voltage AVDD、DVDD	AVDD、DVDD	-0.3 ~ +7	V
Analog Input Voltage to AGND	IAP、IBP、VP	-6 ~ +6	V
Digital Input Voltage to DGND	RX	-0.3 ~ VDD+0.3	V
Digital Output Voltage to DGND	CF, TX	-0.3 ~ VDD+0.3	V
Operating Temperature Range	Topr	-40 ~ +85	℃
Storage Temperature Range	Tstr	-55 ~ +150	℃
Power Dissipation（SOP-16）	P	80	mW

◆ Electronic Characteristic Patameter

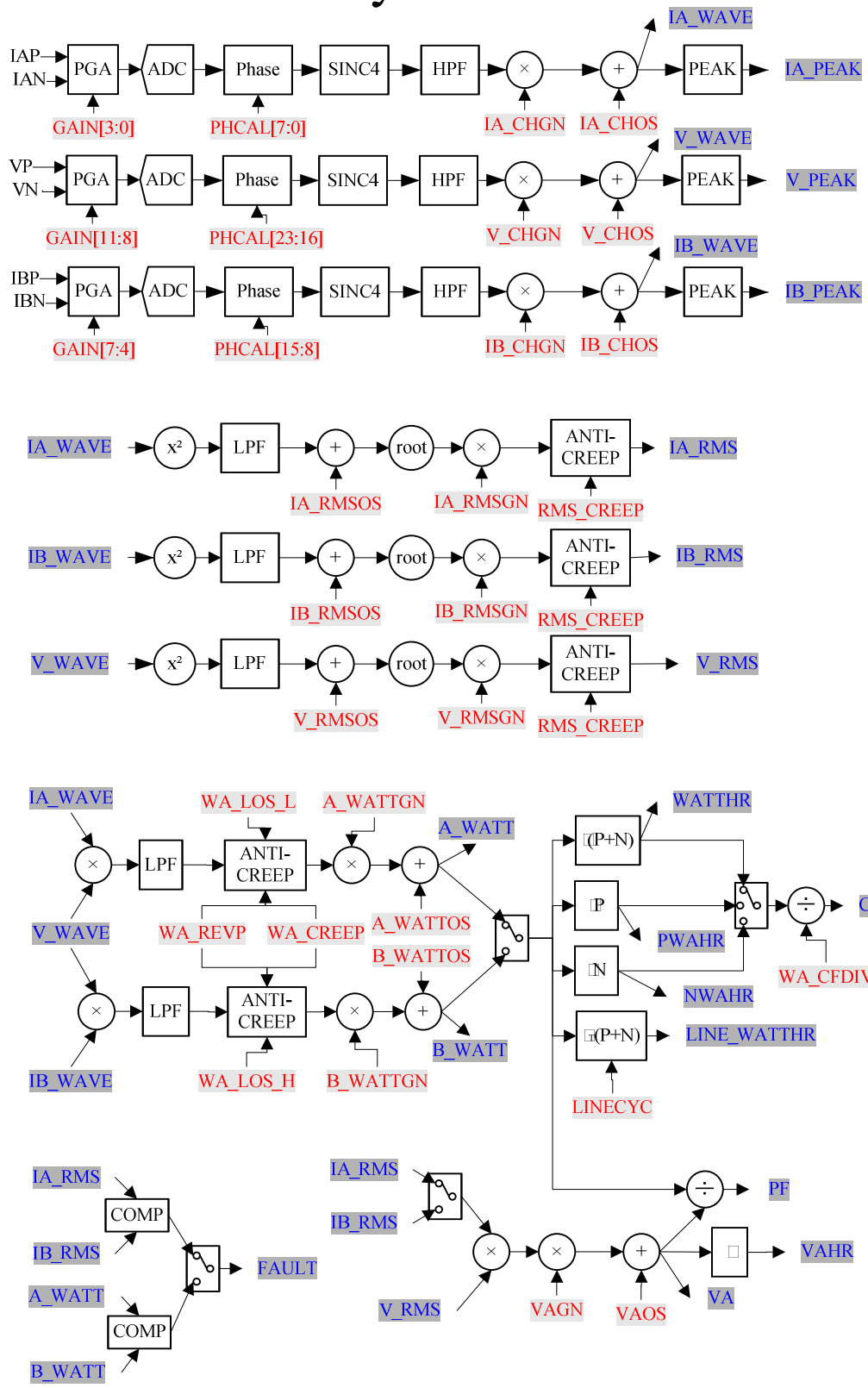
（VDD = 5V, GND = 0V, CLKIN=3.58MHz, T=25℃）

Parameter	Symbol	Test Condition	Measure Pin	Min Value	Typical Value	Max Value	Unit
Measure Error on Active Power	$WATT_{err}$	Over a dynamic range 6000:1	CF		0.1	0.3	%
Phase error when PF=0.8 Capacitive	PF08err	Current lead 37° （PF=0.8）				0.5	%
Phase error when PF=0.5Inductive	PF05err	Current lags 60° （PF=0.5）				0.5	%
AC PSRR	ACPSRR	IP/N=100mV			0.01		%
DC PSRR	DCPSRR	VP/N=100mV			0.1		%
Vrms measurement Error	VRMSerr	3000:1 input DR			0.3		%

Irms measurement Error	IRMSerr	3000:1 input DR			0.3		%
Maximum Input voltage						± 660	mV
Input Impedance				370			kΩ
Input Signal Bandwidth		(-3dB)			14		kHz
Gain Error		External 2.5V reference		-4		+4	%
Gain Error match		External 2.5V reference		-1.5		+1.5	%
On-chip reference	Vref		VREF		2.5		V
Reference Error	Vreferr					± 200	mV
Temperature Coefficient	TempCoef				30		ppm/℃
Input High Voltage		VDD=5V ± 5%		2.6			V
Input Low Voltage		VDD=5V ± 5%				0.8	V
Output High Voltage		VDD=5V ± 5%		4			V
Output Low Voltage		VDD=5V ± 5%				1	V
Power Supply	VDD			4.75		5.25	V
IDD	IDD	VDD=5.25V			5		mA

◆ THEORY OF OPERATION

BL6523GX System Block



◆ Principle of Energy Measurement

In energy measure, the power information varying with time is calculated by a direct multiplication of the voltage signal and the current signal. Assume that the current signal and the voltage signal are cosine functions, V,I are the peak values of the voltage signal and the current signal; the phase difference between the current signal and the voltage signal is expressed as Φ, Then the power is given as follows:

$$p(t) = V\cos(wt) \times I\cos(wt + \Phi)$$

If Φ=0 时:

$$p(t) = \frac{VI}{2}(1 + \cos(2wt))$$

If $\Phi \neq 0$ 时:

$$p(t) = V\cos(wt) \times I\cos(wt + \Phi)$$
$$= V\cos(wt) \times [I\cos(wt)\cos(\Phi) + \sin(wt)\sin(\Phi)]$$
$$= \frac{VI}{2}(1 + \cos(2wt))\cos(\Phi) + VI\cos(wt)\sin(wt)\sin(\Phi)$$
$$= \frac{VI}{2}(1 + \cos(2wt))\cos(\Phi) + \frac{VI}{2}\sin(2wt)\sin(\Phi)$$

p (t) is called as the instantaneous power signal. The ideal p(t) consists of the DC component and AC component whose frequency is 2ω. The DC component is called as the average active power.

The current signal and voltage signal is converted to digital signals by high-precsion ADCS, then through the drop sampling filter (SINC4), high-pass filter (HPF) filter out the high frequency noise and DC gain, get the required current and voltage sampling data.

Current sampling data multiplied by voltage sampling data gets instantaneous active power, then through the low pass filter (LPF), output average active power.

Current sampling data and voltage sampling data processed by square circuit, low-pass filter (LPF1), square root circuit, get the current RMS and voltage RMS.

Active power through a certain time integral, get active energy.

- **Front-end gain adjustment**

Every analog channel has a programmable gain amplifier (PGA), gain selection is achieved by the gain register (GAIN), the default value of the gain register (GAIN) is 000H.

Every 4-bit of the gain register used to select the current channel or voltage channel PGA. Gain[3:0] used to select Current A channel PGA,Gain[7:4] used to select Current B channel PGA, Gain[11:8] used to select Voltage channel PGA.

For example Gain [3:0]:

x000=1x
x001=2x
x010=4x
x011=8x
x100=16x
x101=24x
x110=32x

◆ **Phase compensation**

BL6523GX provides the method of small phase error digital calibration. It will be a small time delay or advance into signal processing circuit in order to compensate for small phase error. Because this compensation should be promptly, so this method applies only to 0.1°~0.5° range of small phase error.

Phase calibration register(PHCAL) is a binary 24-bit register, corresponding to the compensation current A channel, current B channel and voltage channel phase. The default value is 000000H.

PHCAL [23:16] for Voltage channel;

PHCAL [15:8] for Current channel B;

PHCAL [7:0] for Current channel A;

Bit[7]/Bit[15]/Bit[23] is enable bit, when Bit[7] /Bit[15]/Bit[23] ＝ 0,disable Phase compensation; Bit[7]＝1,enable Phase compensation. Bit[6:0]/Bit[14:8]/Bit[22:16] used to adjust the delay time，1.1us/1LSB. With a line frequency of 50Hz, the resolution is 360°×（1/900KHz）×50Hz=0.02°, The adjustable range is 0°~2.54°.

◆ **Input channel offset calibration**

BL6523GX contains the input channel offset calibration registers (IA_CHOS, IB_CHOS, and V_CHOS), these registers are in 16-bit complement format, and the default value is 0000H. The offset may result from the analog input and the analog-digital conversion circuit itself.

◆ **Active power offset calibration**

BL6523GX contains the active power offset calibration (A_WATTOS, B_WATTOS). Both registers are in 16-bit complement format, the default value is 0000H. The offset can exist in the power calculations due to crosstalk between channels on the PCB and in the BL6523GX. The active power offset calibration allows these offsets to be removed to increase the accuracy of the measurement at low input power levels.

$$ActivePower = ActivePower_0 + X\_\mathrm{WATTOS}$$

◆ **Active power gain adjustment**

The gain registers (A_WATTGN, B_WATTGN) are used to adjust the active power measurement range. Both registers are in 16-bit complement format, the default value is 0000H. The following formula shows how to adjust the output active power:

$$Output\ \ ActivePower = Active\ Power \times (1 + \frac{X\_WATTWG}{2^{16}})$$

The minimum value that can be write to the X_WATTGN register is 8001H(HEX), which represents a gain adjustmen of -50%. The maximum value that can be write to the X_WATTGN register is 7FFFH (HEX), which represents a gain adjustmen of +50%.

Similar gain calibration regisets are available for current channel A, current channel B and voltage channel (IA_CHGN, IB_CHGN, V_CHGN).

◆ **No-load threshold of active power**

BL6523GX contains two no-load detection features that eliminate meter creep. BL6523GX can set the no-load threshold on the active power (WA_CREEP), this register is in 24-bit unsign magnitude format. The low 12-bit(WA_CREEP_L) is used to set the active power threshold value,

When the absolute value of the input power signal is less than this threshold, the output active power is set to zero. This can make the active power register to 0 in no-load conditions, even a small noise signal input.

$$WATT = \begin{cases} 0 & , \ |WATT| < WA\_CREEP\_L \\ WATT & , \ |WATT| >= WA\_CREEP\_L \end{cases}$$

The high 12-bit of WA_CREEP register (WA_CREEP_H) is used to set the active power timer threshold value. The default value is 0xFFF. There have an internal TIME_CREEP register in BL6523GX, when detect the CF pulse output, the TIME_CREEP register is set to the value of WA_CREEP_H. If not detected the CF pulse output, the TIME_CREEP register value decrease. If the TIME_CREEP register decrease to 0, there is still no CF signal output, the BL6523GX produce a reset signal used to reset the internal energy accumulated register of CF pulse and reload the value of WA_CREEP_H to the TIME_CREEP register. The resolution of the WA_CREEP_H is 4.6s / LSB, so the maxium timing anti-creep time is about 5h13m.

MODE [6]=1 enable timing anti-creep function.

MODE [6]=0 disable timing anti-creep function.

- **Active power compensation of small signal**

BL6523GX contains a small active power signal compensation register (WA_LOS), this register is in 24-bit format. The default value is 0000H。

WA_LOS [11:0] for current channel A; 12-bit complement format

WA_LOS [23:12] for current channel B; 12-bit complement format

- **Reverse indicator threshold**

BL6523GX contains a reverse indicator threshold register(WA_REVP), this register is in 12-bit unsigned magnitude format, When the input power signal is negative and the absolute value is greater than the power threshold，the BL6523GX output the REVP indicator.

- **Active energy calculation**

The relationship between power and energy can be expressed as：

$$Power = \frac{dEnergy}{dt}$$

Conversely, energy is given as the integral of power.

$$Energy = \int Power \ dt$$

In BL6523GX, the active power signals are accumulated in a 53 internal registers continuously to get active energy, Active energy register WATTHR [23:0] take out this internal register[52:29] as active energy output. This discrete time accumulation is equivalent to integration in continuous time.

$$E = \int p(t)dt = Lim_{T \to 0} \{ \sum_{n=0}^{\infty} P(nT) \times T \}$$

Where:

n is the discrete time-sample number; T is the sampling period; the sampling period of

BL6523GX is 1.1us.

The BL6523GX include a interrupt (APEHF) that is triggered When the active energy register (WATTHR) is half full. If the enable APEHF bit in the interrupt mask register set to logic high, the / IRQ output Pin goes logic low.

The BL6523GX include line cycle energy register (LINE_WATTHR). The number of cycles is writen to the LINECYC register, the LSB of the LINECYC register is 20mS. At the end of a line cycle accumulation cycle, the LINE_WATTHR regiseter is updated. The LINE_WATTHR register hold its current value until the end of the next line cycle period, when the content is replaced with the new reading. If a new value is written to the LINECYC register midway through a line cycle accumulation, the new value is not internally loaded until the end of a line cycle period.

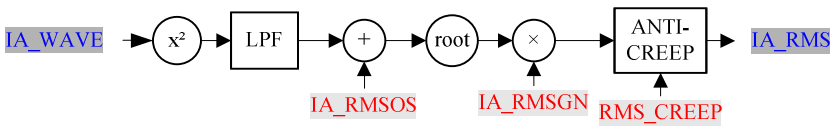
- **Frequency output**

The BL6523GX provides an energy-to-frequency conversion for calibration purpose. After initial calibration at manufacturing, the manufacturer or end customer is often required to verify the meter accuracy. One convenient way to do this is to provide an output frequency that is proportional to the active power. This output frequency provides a simple sigle-wire interface that can be optically isolated to interface to external calibration equipment.

BL6523GX includes a programmable calibration frequency output PIN (CF). The digital-to-frequency converter is used to generate the pulse output. The pulse output (CF) stay high for 90ms if the pulse period is longer than 180ms. If the pulse period is shorter than 180ms, the duty cycle of the pulse output is 50%. The maximum output frequency with ac inputs at full scale and with WA_CFDIV=010H is approximately 0.5 kHz.

The BL6523GX can set the CF frequency through the WA_CF_DIV register. The default value of the WA_CFDIV register is 001H (HEX). When set WA_CFDIV[x]=1, the CF frequency is $2^{(x-4)}*CF_{WA\_CFDIV=010H}$.

- **Root mean square measurement**



The rms is expressed mathematically as:

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T V^2(t)dt}$$

For time-sampled signals:

$$V_{rms} = \sqrt{\frac{1}{N}\sum_{i=1}^{N} V^2(i)}$$

- **rms offset calibration**

BL6523GX contains the rms offset calibration (IA_RMSOS, IB_RMSOS and V_RMSOS). These registers are in 16-bit complement format, the default value is 0000H. The offset can exist in the rms calculations due to input noise that is intergrated in the dc component of square calculation. The rms offset calibration allows these offsets to be removed to increase the accuracy

of the measurement at low input power levels.

$$I_{ARMS} = \sqrt{I_{ARMS0}^{2} + IX\_RMSOS \times 2^{13}}$$

◆ **rms gain calibration**

The gain registers (IA_RMSGN, IB_RMSGN and V_RMSGN) are used to adjust the rms measurement range. Both registers are in 16-bit complement format, the default value is 0000H. The following formula shows how to adjust the rms:

$$Output\ \ rms = rms \times (1 + \frac{X\_RMSGN}{2^{16}})$$

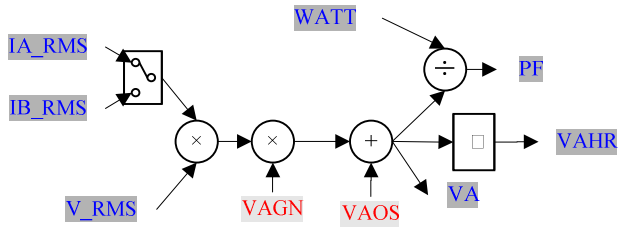
The minimum value that can be write to the X_RMSGN register is 8001H(HEX), which represents a gain adjustment of -50%. The maximum value that can be write to the X_RMSGN register is 7FFFH (HEX), which represents a gain adjustment of +50%.

◆ **No-load threshold of RMS**

BL6523GX can set the no-load threshold on the RMS_CREEP register, this register is in 12-bit unsigned magnitude format. When the value of the RMS register is less than this threshold, the RMS register is set to zero. This can make the RMS register to 0 in no-load conditions, even a small noise signal input.

$$\mathrm{RMS} = \begin{cases} 0 & |RMS| < RMS\_CREEP \times 4/1.3655 \\ \mathrm{RMS}, & |RMS| >= RMS\_CREEP \times 4/1.3655 \end{cases}$$

◆ **Apparent Power and Apparent Energy Calculation**



In BL6523GX, the apparent power is defined as the product of V_RMS and IX_RMS.

VA＝IX_RMS×V_RMS

The apparent energy is given as the intergral of the apparent power. The apparent power signals are accumulated in an internal 49-bit register, apparent energy register VAHR [23:0] take out this internal register [48:25] as apparent energy output. The BL6523GX include a interrupt (VAPEHF) that is triggered When the apparent energy register (VAHR) is half full. If the enable VAPEHF bit in the interrupt mask register set to logic high, the / IRQ output Pin goes logic low.

◆ **Power Factor**

PF＝ (WATT/VA)

PF register is in 24-bit sign magnitude format. Power factor =(sign bit)*((PF[22]×2^－1）＋（PF[21]×2^－2）＋。。。), the register value of 0x7FFFFF(HEX) corresponds to a power factor value of 1, the register value of 0x800000(HEX) corresponds to a power factor of -1, the register value of 0x400000(HEX) corresponds to a power factor of 0.5.

◆ Operation Mode Select

◆ Metering channel selection

The default metering channel of BL6523GX is channel A. the MODE [0] of MODE register is used to select the metering channel.

MODE[0]=0, the metering channel is channel A;

MODE[0]=1, the metering channel is channel B;

MODE[1]=0; disable auto channel select;

MODE[1]=1; enable auto channel select; when the chip detect the imbalance of two current channel, the chip select the bigger current channel as the metering channel.

◆ High-pass filter selection

In the analog-digital conversion circuit, the current and voltage channels have high-pass filters to eliminate the DC offset. The MODE [4:2] of MODE register is used to select high-pass filter.

MODE [2] =0, enable the high-pass filter of current channel A;

MODE [2] =1, disable the high-pass filter of current channel A;

MODE [3] =0, enable the high-pass filter of current channel B;

MODE [3] =1, disable the high-pass filter of current channel B;

MODE [4] =0, enable the high-pass filter of voltage channel;

MODE [4] =1, disable the high-pass filter of voltage channel;

◆ Energy accumulation mode selection

The MODE[9:8] of the MODE regiset is used to select energy accumulation mode.

MODE[9:8]=00, absolute energy accumulation;

MODE[9:8]=01, positive-only energy accumulation;

MODE[9:8]=10, arithmetical energy accumulation;

MODE[9:8]=11, negative-only energy accumulation;;

◆ The current imbalance judgment

The BL6523GX contains the detection of current imbalance. MODE[11:10] of the MODE register is used to set the current rms imbalance threshold. When the Line current rms and neutral current rms difference exceeds the threshold, the BL6523GX give the FAULT indicator.

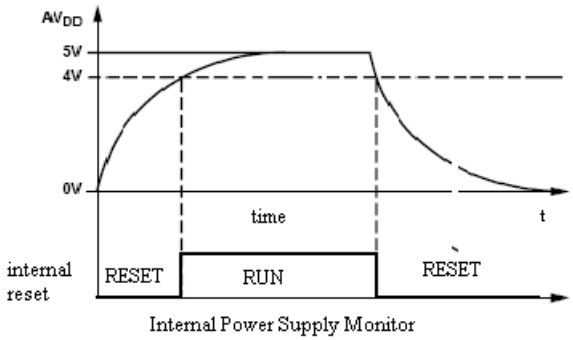
MODE[11]	MODE[10]	Threshold
0	0	12.5%(default)
0	1	6.25%
1	0	3.125%
1	1	10.1%

◆ Electric parameters monitor

◆ Power Supply Monitor

The BL6523GX contains an on-chip power supply monitor. The power supply (VDD) is continuously monitored by the BL6523GX. if the supply is less than 4V±5%, the BL6523GX will be reset. This is useful to ensure correct device startup at power-up and power-down. The power supply monitor has built in hysteresis and filtering. This gives a high degree of immunity to

false triggering due to noisy supplies. The power supply and decoupling for the part should be such that the ripple at AVDD does not exceed 5V±5% as specified for normal operation.



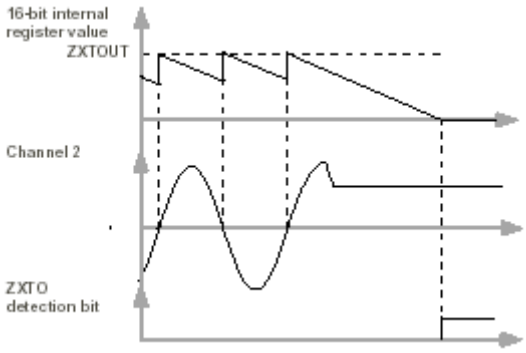
Internal Power Supply Monitor

◆ **Zero-Crossing Detection**

The BL6523GX includes a zero-crossing detection on voltage channel. The ZX output pin goes high on positive-going edge of the voltage channel zero crossing.

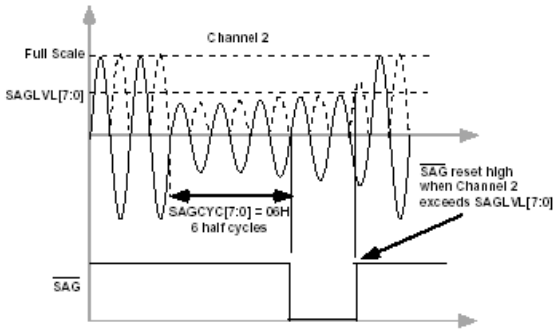
◆ **Zero-Crossing Timeout**

The BL6523GX includes a zero-crossing timeout feature that is designed to detect when no zero crossings are obtained over a programmable time period. The duration of the zero-crossing timeout is programmed in the 16-bit ZXTOUT register. The value in the ZXTOUT register is decremented by 1LSB every 70.5us. If a zero-crossing is obtained, the ZXTOUT register is reloaded. If the ZXTOUT register reaches 0, a zero-crossing timeout event is issued. The maximum programmable timeout period is 4.369 secs. An interrupt is associated with the zero-crossing timeout feature. If enabled, a zero-crossing timeout event causes the external IRQ pin to go low.



◆ **Voltage Sag Detection**

The BL6523GX includes a sag detection features that warns the user when the absolute value of the line voltage falls below the programmable threshold for a programmable number of half line cycles. The voltage sag feature is controlled by two registers: SAGLVL and SAGCYC. These registers control the sag voltage threshold and the sag period, respectively.



The 12-bit SAGLVL register contains the amplitude that the voltage channel must fall below before sag event occurs.The sag threshold is the number of half line cycles below which the voltage channel must remain before a sag condition occurs. Each LSB of the SAGCYC register corresponds to one half line cycle period. The default value is 0xFF(HEX). At 50Hz, the maximum sag cycle time is 2.55 seconds.

- **Peak Detection**

The BL6523GX continuously records the maximum value of the current and voltage channels. The three registers that record the peak values on current channel A, current channel B, and the voltage channel, respectively, are IA_PEAK, IB_PEAK and V_PEAK.

- **Peak monitor**

The BL6523GX include an overcurrent and overvoltage feature that detects whether the absolute value of the current or voltage waveform exceeds a programmable threshold. Three peak threshold register (I_PKLVL and V_PKLVL) are used to set the current or voltage channel peak threshold, respectively.

If the BL6523GX detects an overvoltage condition, the PKV bit of the interrupt status register is set to 1. If the PKV bit of the interrupt mask register is enable, the IRQ output go low. The overcurrent detection feature works in the similar manner.

Interrupt

The BL6523GX uses interrupt status register and interrupt mask register to manage interrupts. When an interrupt event occurs, the corresponding bit in the STATUS register is set to 1. If the enable bit for this interrupt, located in the MAK register is set to 0, the external IRQ pin is pulled to logic 0. The status bit located in the STATUS register is set when an interrupt event occurs, regardless of whether the external interrupt is enabled.

All interrupts are latched and require servicing to clear. To service the interrupt and return the IRQ pin to logic 1, the status bits must be cleared using the STATUS register. After completion of a read from the STATUS register, the IRQ pin returns to logic 1.the status bit can't be cleared after a read operation of STAUTS register, but can be writen 0 to the corresponding bit in the status register through the SPI interface clearing the status bit.

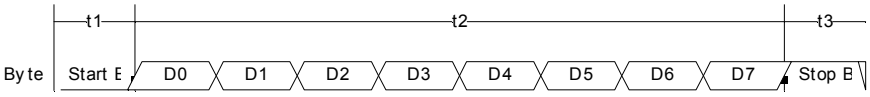
UART interface

The BL6523GX provides a simple UART interface that allows all the functions of BL6523GX to be accessed using only two single-diredtion pins. This UART interface allows an

isolated communication interface to be achieved using only two low cost opto-isolators.

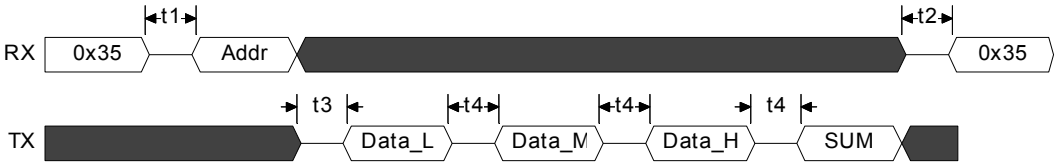
The baud rate is 4800 bps, No parity, 1 stop bit.

Byte format:



t1=t3=208uS; t2=208*8=1664uS.

Read register frame：

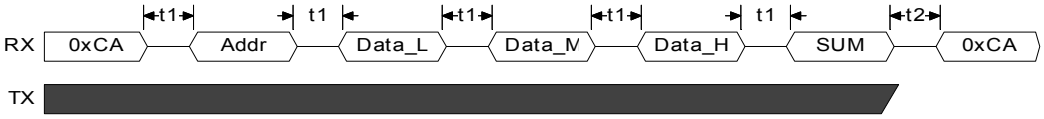


0x35: Read command byte;

Addr: BL6523GX register address;

SUM:（Addr+Data_L+Data_M+Data_H）&0xFF, then byte invert;

Write register frame:



0xCA: write command byte;

Addr: BL6523GX register address;

SUM:（Addr+Data_L+Data_M+Data_H）&0xFF, then byte invert;

◆ Register

◆ Register list

ADDRESS	REGISTER NAME	EXTERNAL R/W	INTERNAL R/W	BIT	DEFAULT	DESCRIPTION
ELECTRIC PARAMETERS REGISTER（INTERNAL WRITE）						
01H	IA_WAVE	R	W	24	0	Wave register of channel A
02H	IB_WAVE	R	W	24	0	Wave register of channel B
03H	V_WAVE	R	W	24	0	Wave register of Voltage
04H	LINE_ WATTHR	R	W	24	0	Line cycle energy register
05H	IA_RMS	R	W	24	0	Irms register(channel A)
06H	IB_RMS	R	W	24	0	Irms register(channel B)
07H	V_RMS	R	W	24	0	Vrms
08H	PF	R	W	24	0	Power Factor
09H	FREQ	R	W	24	0	Frequency register
0AH	A_WATT	R	W	24	0	Average active power of channel A
0BH	VA	R	W	24	0	Average apparent power
0CH	WATTHR	R	W	24	0	Active energy
0DH	VAHR	R	W	24	0	Apparent energy
0EH	PWAHR	R	W	24	0	Positive active energy
0FH	NWAHR	R	W	24	0	Negative active energy
10H	IA_PEAK	R	W	24	0	Current A Peak register
11H	IB_PEAK	R	W	24	0	Current B Peak register
12H	V_PEAK	R	W	24	0	Voltage Peak register
13H	B_WATT	R	W	24	0	Average active power of channel B
Calibration registers (External write，Except 3AH）						
14H	MODE	R/W	R	24	000000H	Mode regiser,
15H	GAIN	R/W	R	12	000H	Channel Gain register
16H	FAULTLVL	R/W	R	12	044H	Current imbalance shielding threshold register
17H	WA_CREEP	R/W	R	24	FFF02BH	Active power no-load threshold register
18H	WA_REVP	R/W	R	12	087H	Reverse threshold register
19H	WA_CFDIV	R/W	R	12	001H	Active power CF frequency divider
1AH	A_WATTOS	R/W	R	16	0	Active power offset correction(current channel A)
1BH	B_WATTOS	R/W	R	16	0	Active power offset correction(current B)

1CH	A_WATTGN	R/W	R	16	0	Active power gain(current channel A)
1DH	B_WATTGN	R/W	R	16	0	Active power gain(current channel B)
1EH	FREQ_SEL	R/W	R	16	4924H	Analog circuitry Frequency Control
1FH	BG_CTRL	R/W	R	16	0F33H	Analong circuitry Control
20H	PHCAL	R/W	R	24	0	Phase calibration register
21H	VAOS	R/W	R	16	0	Apparent Power Offset Calibration Register
22H	VAGN	R/W	R	16	0	Apparent power gain adjust register
23H	IA_RMSGN	R/W	R	16	0	Current A RMS gain adjust register
24H	IB_RMSGN	R/W	R	16	0	Current B RMS gain adjust register
25H	V_RMSGN	R/W	R	16	0	Voltage RMS gain adjust register
26H	IA_RMSOS	R/W	R	16	0	Current A RMS Offset Calibration register
27H	IB_RMSOS	R/W	R	16	0	Current B RMS Offset Calibration register
28H	V_RMSOS	R/W	R	16	0	Voltage RMS Offset Calibration register
29H	RMS_CREEP	R/W	R	12	0	RMS small signal threshold register
2AH	WA_LOS	R/W	R	24	0	Active-power offset Calibration register Bit[23:12] B channel; Bit[11:0] A channel;
2BH	IA_CHOS	R/W	R	16	0	Current A channel offset adjustment register，
2CH	IB_CHOS	R/W	R	16	0	Current B channel offset adjustment register
2DH	V_CHOS	R/W	R	16	0	Voltage channel offset adjustment register
2EH	IA_CHGN	R/W	R	16	0	Current A channel gain adjustment register
2FH	IB_CHGN	R/W	R	16	0	Current B channel gain adjustment register
30H	V_CHGN	R/W	R	16	0	Voltage channel gain adjustment register
31H	LINECYC	R/W	R	12	000H	Line energy accumulation cycles register
32H	ZXTOUT	R/W	R	16	FFFFH	Zero-crossing timeout
33H	SAGCYC	R/W	R	8	FFH	Sag period
34H	SAGLVL	R/W	R	12	0	Sag voltage level
35H	Reversed					
36H	I_PKLVL	R/W	R	24	FFFFFFH	Current peak threshold
37H	V_PKLVL	R/W	R	12	FFFH	Voltage peak threshold
38H	AT_SEL	R/W	R	16	0	Logic output selection

39H	MASK	R/W	R	16	0	Interrupt mask register,
3AH	STATUS	R	W	16	0	Interrupt state register
Special register						
3BH	READ	R	R	24	0	Contains the data from the last read operation of SPI
3CH	WRITE	R	R	24	0	Contains the data from the last write operation of SPI
3DH	CHKSUM	R	R	24	015A4AH	Checksum。The sum of register 14H~39H(except 35H)
3EH	WRPROT	R/W	R	8	0	Write protection register. Write 55H, it means that allows write to writable register。
3FH	SOFT_NRST	R/W	/	24		Write 5A5A5AH to this register, Reset BL6523GX

◆ **Logic output selection register(AT_SEL)**

The BL6523GX contains four logic output pin(AT0~AT3) that can output some measurement states. The AT_SEL register is used to set the AT0~AT3 pin output, AT_SEL [3：0] corresponds to AT0; AT_SEL[7：4] corresponds to AT1; AT_SEL[11：8] corresponds to AT2; AT_SEL[15：12] corresponds to AT3. The default value of AT_SEL register is 0x0000, the default output is AT0=FAULT, AT1=REVP, AT2=ZX, AT3=nSAG.

设置	ATX OUTPUT	DEFAULT	DESCRIPTION
0000			AT0=FAULT、AT1=REVP、AT2=ZX、AT3=nSAG
0001	nSAG	0	Sag event has occurred
0010	ZXTO	0	Indicates that zero crossing has been missing on the voltage channel for the length of time specified in the ZXTOUT register
0011	ZX	0	Voltage channel zero crossing
0100	PKIA	0	Current channel A peak has exceeded IAPKLVL
0101	PKIB	0	Current channel B peak has exceeded IBPKLVL
0110	PKV	0	Voltage peak has exceeded VPKLVL
0111	REVP	0	Sign of active power has changed to negative
1000	APEHF	0	Active energy register(WATTR) is half full
1001	VAPEHF	0	Apparent energy register(VAHR) is half full
1010	FAULT	0	Fault=1 indicates the imbalance in two channels rms, the difference is greater than the FAULTLVL
1011	CHSEL	0	0 indicates measureing power with channel A; 1 indicates measureing power with channel B;
其余	Reversed	0	Reserved

◆ **Interrupt mask register（MASK）**

BITS	INTERRUP	DEFAULT	DESCRIPTION

	NAME		
0	SAG	0	Enable the interrupt that sag event has occurred
1	ZXTO	0	Enable the interrupt of ZXTO
2	ZX	0	Enable the interrupt of ZX
3	PKIA	0	Enable the interrupt of PAIA
4	PKIB	0	Enable the interrupt of PKIB
5	PKV	0	Enable the interrupt of PKV
6	REVP	0	Enable the interrupt of REVP
7	APEHF	0	Enable the interrupt of APEHF
8	VAPEHF	0	Enable the interrupt of VAPEHF
9	FAULT	0	Enable the interrupt of FAULT
10	CHSEL	0	Enable the interrupt of CHSEL
Others	Reversed	0	Reversed

◆ **Interrupt status registers(STATUS)**

BITS	BIT NAME	DEFAULT	DESCRIPTION
0	SAG	0	Sag event has occurred
1	ZXTO	0	Indicates that zero crossing has been missing on the voltage channel for the length of time specified in the ZXTOUT register
2	ZX	0	Voltage channel zero crossing
3	PKIA	0	Current channel A peak has exceeded IAPKLVL
4	PKIB	0	Current channel B peak has exceeded IBPKLVL
5	PKV	0	Voltage peak has exceeded VPKILVL
6	REVP	0	Sign of active power has changed to negative
7	APEHF	0	Active energy is half full
8	VAPEHF	0	Apparent energy is half full
9	FAULT	0	Fault=1 indicates the imbalance in two channels rms, the difference is greater than the FAULTLVL
10	CHSEL	0	0 indicates measureing power with channel A; 1 indicates measureing power with channel B;
Others	Reversed	0	Reserved